4. (Amended) A semiconductor device comprising a delay locked loop including:

an input buffer receiving an external clock and outputting a first internal clock;

a delay circuit delaying said first internal clock to output a second internal clock;

a detector detecting which of said first and second clocks is advanced in a phase; and

a gray code counter using a gray code, responsive to an output of said detector for generating a signal to increase or decrease an amount of delay of said delay circuit.

11. (Amended) A semiconductor device comprising a delay locked loop including:

a first input buffer receiving at least a first external clock and a second external clock complementary in phase to said first external clock, and outputting a first internal clock at the timing of the rising edge of said first external clock when a potential of said first external clock is equal to that of said second external clock;

a second input buffer receiving at least said first and second external clocks, and outputting a second internal clock at the timing of the rising edge of said second external clock when a potential of said first external clock is equal to that of said second external clock;

a first delay circuit delaying said first internal clock to output a third internal clock;

a second delay circuit delaying said second internal clock to output a fourth internal clock;

a detector detecting which of said first and second clocks is advanced in a phase; and

a gray code counter using a gray code, responsive to an output of said detector for generating a signal to increase or decrease an amount of delay of said first delay circuit and an amount of delay of said second delay circuit.

14. (Amended) A control method for a system operating in synchronization with a clock, comprising the steps of:

inputting an external clock to an input buffer to generate a first internal clock therefrom;

delaying said first internal clock to output a second internal clock;

detecting which of said first and second clocks is advanced in a phase; and

using a gray code to increase or decrease an amount of delay to be applied in the step of delaying, said amount of delay corresponding to a result obtained in the step of detecting.